UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

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KATSUHISA OGAWA	
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APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

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1. [ ] Fee Transmittal Form *(Submit an original, and a duplicate for fee processing)*
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ACCOMPANYING APPLICATION PARTS

8. [ ] Assignment Papers (cover sheet & document(s))
9. [ ] 37 CFR 3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [ ] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
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	INDEPENDENT CLAIMS (37 cfr 1 16(b))	2-3 =	0	X $ 78.00 =	$ -0-
	MULTIPLE DEPENDENT CLAIMS (if applicable) (37 CFR 1.16(d))			$260.00 =	$ -0-
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a. ☐ A Small entity statement is enclosed

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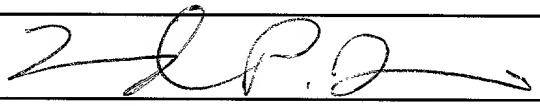
NAME	Leonard P. Diana (29,296)
SIGNATURE	
DATE	December 11, 1998

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Image Pickup Element

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to an image pickup element for outputting an arbitrary image region and an image pickup device for interpolating an arbitrary image region.

Related Background Art

In an image pickup device, to obtain a color image from a single image pickup element, light is incident on the image pickup element through color filter arrays. Color filter arrays are roughly classified into a primary color filter array and a complementary color filter array. In a primary color filter array, three filters, i.e., an R filter for transmitting only red light within the visible light range, a G filter for transmitting only green light within the visible light range, and a B filter for transmitting only blue light within the visible light range are arrayed in, e.g., a matrix. In a complementary color filter array, a cyan (to be referred to as "Cy" hereinafter) filter for shielding only red light within the visible light range, a magenta (to be referred to as "Mg" hereinafter) filter for shielding only green light within the visible light range, and a yellow (to be referred to as "Ye" hereinafter) filter for shielding

only blue light within the visible light range are arrayed in, e.g., a matrix. There are various color filter array patterns. Fig. 1 shows an example of the primary color filter array. This is called a Bayer matrix.

The Bayer matrix will be described. Of the basic units of the array pattern of 2 × 2 color filters, only the upper left pixel can directly output a red signal from a photoelectric conversion element as a detection unit of an image pickup element. Only the upper right and lower left pixels can output a green signal, and only the lower right pixel can output a blue signal. To obtain the respective color signals from these pixels, interpolation processing is required. In interpolation, the value of a pixel to be interpolated is obtained by signal processing or calculation based on the values of the neighboring pixels.

Figs. 2A to 2C are views for explaining an example of interpolation corresponding to the Bayer matrix shown in Fig. 1. Symbol ○ indicates an original pixel obtained from a photoelectric conversion element. Symbol △ indicates an interpolated pixel obtained by interpolation. An arrow indicates the relationship between an interpolated pixel and its original pixel.

Fig. 3 is a block diagram of a conventional single-plate color image pickup device. Referring to Fig. 3, the device comprises a CCD image pickup element

901, an A/D converter (ADC) 902, a memory 903, an interpolation circuit 904, a signal processing circuit 905, and a D/A converter (DAC) 906. The memory 903 requires a capacity corresponding to the number of bits of at least (two lines + two pixels) × ADC. The memory 903 is constituted by, e.g., a FIFO having an output terminal at its middle point.

In the CCD image pickup element 901, a photodetection signal obtained by each photoelectric conversion element is transferred in the vertical direction by a CCD and then transferred in the horizontal direction by a CCD. More specifically, when all photodetection signals of a certain line are transferred by the vertical CCD to reach the horizontal CCD, all the photodetection signals are sequentially transferred in the horizontal direction by the horizonal CCD and output from an output terminal. This operation is sequentially performed for all lines. Therefore, photodetection signals (original pixels) are output from the CCD image pickup element 901 in the order of scanning lines, as shown on the CCD image pickup element 901 in Fig. 3.

Each original pixel output from the CCD image pickup element 901 is A/D-converted by the ADC 902 and stored in the memory 903. A plurality of original pixels on each of the first, second, and third lines output from the memory 903 are input to the

interpolation circuit 904. The interpolation circuit 904 interpolates as shown in Figs. 2A to 2C on the basis of these original pixels and outputs RGB signals interpolated by the interpolated pixels. The signal processing circuit 905 processes the RGB signals by color gain adjustment or edge enhancement. The DAC 906 D/A-converts the processed RGB signals to output analog RGB signals.

In the above-described prior art, interpolated pixels must be obtained on the basis of original pixels output from the CCD image pickup element 901 in the order of scanning lines. For this purpose, the ADC 902, memory 903, and DAC 906 are required in addition to the interpolation circuit 904 and signal processing circuit 905, resulting in an increase in circuit scale.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide an image pickup element capable of outputting a signal from a pixel in an arbitrary basic block.

It is an another object of the present invention to provide an image pickup element capable of outputting a signal from a pixel in an arbitrary basic block which is appropriate to calculation of interpolated pixel.

It is an another object of the present invention to provide an image pickup device capable of reducing

circuit scale.

It is another object of the present invention to provide an image pickup device capable of obtaining an interpolated pixel without any A/D converter, memory for a plurality of lines, and D/A converter.

In order to achieve the above object, according to an aspect of the present invention, there is provided an image pickup element comprising a plurality of photodetectors each having a color filter array, vertical direction selection means for selecting in a vertical direction an arbitrary basic block having at least two of the plurality of photodetectors, horizontal direction selection means for selecting the arbitrary basic block in a horizontal direction, and output means for parallelly outputting outputs from the photodetectors in the arbitrary basic block selected by the vertical direction selection means and the horizontal direction selection means.

According to another aspect of the present invention, there is provided an image pickup device comprising:

(A) an image pickup element including;

(a) a plurality of photodetectors each having a color filter array;

(b) vertical direction selection means for selecting in a vertical direction an arbitrary basic block having at least two of the plurality

of photodetectors;

(c) horizontal direction selection means for selecting the arbitrary basic block in a horizontal direction; and

(d) output means for parallelly outputting outputs from the photodetectors in the arbitrary basic block selected by the vertical direction selection means and the horizontal direction selection means;

(B) block storage means for storing a plurality of outputs from the image pickup elements in units of basic blocks; and

(C) interpolation means for calculating an interpolated pixel on the basis of an output from the block storage means.

By the image pickup element having the above arrangement, processing on the output side is facilitated.

In addition, by the above image pickup device, the circuit scale can be reduced.

Other objects, features, and advantages of the present invention will be apparent from the following specification and accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a view showing the basic pattern of a color filter array in a Bayer matrix;

Figs. 2A, 2B and 2C are views for explaining an example of interpolation of RGB signals corresponding to the Bayer matrix;

Fig. 3 is a block diagram showing the arrangement of a conventional single-plate color image pickup device;

Fig. 4 is a block diagram showing the arrangement of a single-plate color image pickup device according to the present invention;

Fig. 5 is a first view for explaining interpolation processing according to the first embodiment of the present invention;

Fig. 6 is a second view for explaining interpolation processing according to the first embodiment of the present invention;

Fig. 7 is a view showing the basic pattern of a complementary color filter array;

Fig. 8 is a first view for explaining interpolation processing according to the second embodiment of the present invention;

Fig. 9 is a second view for explaining interpolation processing according to the second embodiment of the present invention;

Fig. 10 is a third view for explaining interpolation processing according to the second embodiment of the present invention;

Fig. 11 is a block diagram showing the arrangement

of an image pickup element according to the third embodiment of the present invention; and

Fig. 12 is a block diagram showing the arrangement of an image pickup element according to the fourth embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In embodiments to be described below, an image pickup element such as so-called CMOS image pickup element capable of reading a pixel at an arbitrary portion at random is used.

Fig. 4 is a block diagram showing the arrangement of an image pickup device according to the first embodiment. Referring to Fig. 4, the image pickup device comprises an image pickup element 101, a block memory 102, an interpolation circuit 103, and a signal processing circuit 104.

Original pixels are read from the image pickup element 101 in units of 2 × 2 basic (minimum) blocks of a Bayer matrix. The block memory 102 stores read original pixels of a plurality of basic blocks. In this embodiment, the block memory 102 stores three basic blocks in the horizontal direction and three basic blocks in the vertical direction, i.e., a total of nine basic blocks. The interpolation circuit 103 interpolates as shown in Figs. 2A to 2C on the basis of the original pixels stored in the block memory 102 and

outputs interpolated RGB signals. The signal processing circuit 104 processes the interpolated RGB signals by color gain adjustment, low-frequency filtering, or edge enhancement and outputs the processed RGB signals. The signals obtained from the image pickup element 101 and output from the signal processing circuit 104 are analog signals.

The block memory 102, interpolation circuit 103, and signal processing circuit 104 are formed on one chip together with the image pickup element 101. For example, when the image pickup element 101 is a CMOS image pickup element, the image pickup element 101, block memory 102, interpolation circuit 103, and signal processing circuit 104 are formed on one chip by the same CMOS process.

Fig. 5 is a view showing the array of original pixels stored in the block memory 102. Referring to Fig. 5, symbols A, B, C, D, E, F, G, H, I, J, K, L, M, N, P, and Q denote basic blocks. The block memory 102 simultaneously stores 3 × 3 basic blocks, as indicated by reference numeral 20 in Fig. 5.

Fig. 6 is a view for explaining interpolation processing by the interpolation circuit 103. The interpolation circuit 103 generates interpolated pixels pointed by arrowheads in Fig. 6 on the basis of the original pixels stored in the block memory 102, which are indicated by reference numeral 20 in Fig. 5, in

accordance with the following equations exemplifying the basic block F:

$$R_{F2} = (R_{F1} + R_{G1})/2$$

$$R_{F3} = (R_{F1} + R_{J1})/2$$

$$R_{F4} = (R_{F1} + R_{K1})/2$$

$$G_{F1} = (G_{E2} + G_{F2})/2$$

$$G_{F4} = (G_{F3} + G_{G3})/2$$

$$B_{F1} = (B_{A4} + B_{F4})/2$$

$$B_{F2} = (B_{B4} + B_{F4})/2$$

$$B_{F3} = (B_{E4} + B_{F4})/2$$

When interpolation of the basic block F is complete, the basic blocks D, H, and L are read from the image pickup element 101 and written in the block memory 102. The basic blocks A, E, and I are erased from the block memory 102. The interpolation circuit 103 generates the interpolated pixels of the basic block G on the basis of the original pixels of the basic blocks B, C, D, F, G, H, J, K, and L in the same manner as described above.

By repeating the block reading and interpolation, the interpolation circuit 103 outputs interpolated RGB signals in the order of, e.g., the basic blocks F, G, H,..., J, K, L,..., N, P, Q,.... However, the basic block output order is not limited to this. For example, when block processing such as calculation of the discrete cosine transforms (DCTs) of 8 × 8 pixels is to be done on the output side of the signal

processing circuit, the signals can be read in the order of the basic blocks F, G, J, K,.... to continuously output 8 × 8 pixel data. The basic block size may be equal to the block processing size.

An image pickup device according to the second embodiment has the same arrangement as that of the first embodiment shown in Fig. 4. In the second embodiment, a complementary color filter array is used as a color filter array. The arrangement of the image pickup device of the second embodiment is the same as that of the first embodiment shown in Fig. 4, and a detailed description thereof will be omitted.

Fig. 7 is a view showing the basic pattern of the complementary color filter array in this embodiment. Referring to Fig. 7, the basic pattern has a size of 4 lines × 2 pixels.

The basic block size in block reading of this embodiment is the same as in the first embodiment, i.e., 2 × 2 pixels. The basic pattern of the color filter array is different from the basic block in block reading.

Fig. 8 is a view showing the array of original pixels stored in a block memory 102. Referring to Fig. 8, symbols A, B, C, D, E, F, G, H, I, J, K, L, M, N, P, and Q denote basic blocks. The block memory 102 simultaneously stores 3 × 3 basic blocks, as indicated by reference numeral 40 or 50 in Fig. 8.

Figs. 9 and 10 are views for explaining interpolation processing by an interpolation circuit 103. Fig. 9 shows interpolation processing for basic blocks at an upper portion 201 of the basic pattern shown in Fig. 7. Fig. 10 shows interpolation processing for basic blocks at a lower portion 202 of the basic pattern shown in Fig. 7. Referring to Fig. 8, the basic blocks A, B, C, D, I, J, K, and L correspond to the upper portion 201, and the basic blocks E, F, G, H, M, N, P, and Q correspond to the lower portion 202.

For the basic blocks at the upper portion 201, the interpolation circuit 103 generates interpolated pixels pointed by arrowheads in Fig. 9 on the basis of the original pixels stored in the block memory 102, which are indicated by reference numeral 40 in Fig. 8, in accordance with the following equations exemplifying the basic block J:

$$Cy_{J2} = (Cy_{J1} + Cy_{K1})/2$$

$$Cy_{J3} = (Cy_{J1} + Cy_{N1})/2$$

$$Cy_{J4} = (Cy_{J1} + Cy_{P1})/2$$

$$Ye_{J1} = (Ye_{I2} + Ye_{J2})/2$$

$$Ye_{J3} = (Ye_{J2} + Ye_{M2})/2$$

$$Ye_{J4} = (Ye_{J2} + Ye_{N2})/2$$

$$Mg_{J3} = (Mg_{I4} + Mg_{J4})/2$$

$$Mg_{J1} = (Mg_{F3} + Mg_{J3})/2$$

$$Mg_{J2} = (Mg_{G3} + Mg_{J3})/2$$

$$G_{J4} = (G_{J3} + G_{K3})/2$$

$$G_{J1} = (G_{E4} + G_{J4})/2$$

$$G_{J2} = (G_{F4} + G_{J4})/2$$

For the basic blocks at the lower portion 202, the interpolation circuit 103 generates interpolated pixels pointed by arrowheads in Fig. 10 on the basis of the original pixels stored in the block memory 102, which are indicated by reference numeral 50 in Fig. 8, in accordance with the following equations exemplifying the basic block F:

$$Cy_{F2} = (Cy_{F1} + Cy_{G1})/2$$

$$Cy_{F3} = (Cy_{F1} + Cy_{I1})/2$$

$$Cy_{F4} = (Cy_{F1} + Cy_{K1})/2$$

$$Ye_{F1} = (Ye_{E2} + Ye_{F2})/2$$

$$Ye_{F3} = (Ye_{F2} + Ye_{I2})/2$$

$$Ye_{F4} = (Ye_{F2} + Ye_{J2})/2$$

$$Mg_{F4} = (Mg_{F3} + Mg_{G3})/2$$

$$Mg_{F1} = (Mg_{A4} + Mg_{F4})/2$$

$$Mg_{F2} = (Mg_{B4} + Mg_{F4})/2$$

$$G_{F3} = (G_{E4} + G_{F4})/2$$

$$G_{F1} = (G_{B3} + G_{F3})/2$$

$$G_{F2} = (G_{C3} + G_{F3})/2$$

The interpolation circuit 103 switches the two interpolation modes in accordance with the type of basic blocks. The original pixels are read from an image pickup element 101 and written in the block memory in the same manner as in the first embodiment.

By repeating the block reading and interpolation, the interpolation circuit 103 outputs interpolated CyMgYe signals in the order of, e.g., the basic blocks F, G, H,..., J, K, L,..., N, P, Q,.... However, the basic block output order is not limited to this. For example, when the DCTs of 8 × 8 pixels are to be calculated on the output side of the signal processing circuit, the signals can be read in the order of the basic blocks F, G, J, K,.... to continuously output 8 × 8 pixel data.

The arrangement of the image pickup element 101 will be described next. Fig. 11 is a block diagram showing the arrangement of an image pickup element 101 in the third embodiment.

Referring to Fig. 11, the image pickup element comprises photodetectors 301 such as photodiodes, a vertical direction (row direction) read-out block selection circuit 302, a horizontal direction (column direction) read-out block selection circuit 303, transfer switches 304, vertical direction block selection lines 305, horizontal direction block selection lines 306, and output lines 307. The output lines are connected to an output terminal.

For the vertical direction block selection lines 305 equal in number to the basic blocks in the vertical direction, the vertical direction read-out block selection circuit 302 activates only lines of selected

blocks. Similarly, for the horizontal direction block selection lines 306 equal in number to the basic blocks in the horizontal direction, the horizontal direction read-out block selection circuit 303 activates only lines of selected blocks. Each photodetector 301 outputs a detection signal only when both the vertical direction block selection line 305 and horizontal direction block selection line 306 are activated. Each of the transfer switches 304 equal in number to the basic blocks in the horizontal direction receives the detection signal when any one of the basic blocks 301 of a line to which the transfer switches 304 belong outputs a detection signal. The outputs from the transfer switches 304 are coupled and sent to the output terminal. Since one of the outputs is selected by the horizontal direction block selection lines 306, only the detection signal from the basic block selected by the vertical direction block selection line 305 and horizontal direction block selection line 306 is output from the output terminal.

When the vertical direction read-out block selection circuit 302 and horizontal direction read-out block selection circuit 303 are simultaneously operated, the detection signal from an arbitrary basic block can be output from the output terminal.

Fig. 12 is a block diagram showing the arrangement of an image pickup element 101 according to the fourth

embodiment.

Referring to Fig. 12, the device comprises photodetectors 401 such as photodiodes, a vertical direction (row direction) read-out block selection circuit 302, a horizontal direction (column direction) read-out block selection circuit 303, a two-line memory 402, vertical direction photodetector selection lines 403, horizontal direction block selection lines 306, and output lines 307. The output lines are connected to an output terminal. The vertical direction read-out block selection circuit 302, horizontal direction read-out block selection circuit 303, vertical direction block selection lines 305, and horizontal direction block selection lines 306 are the same as those of the third embodiment.

For the vertical direction photodetector selection lines 403 equal in number to the photodetectors in the vertical direction, the vertical direction read-out block selection circuit 302 activates only lines of selected blocks. Since the outputs from photodetectors on one line are output to the same line, the lines are sequentially activated. For the horizontal direction block selection lines 306 equal in number to the basic blocks in the horizontal direction, the horizontal direction read-out block selection circuit 303 activates only lines of selected blocks. Each photodetector 401 outputs a detection signal only when

a corresponding vertical direction photodetector selection line 403 is activated. The two-line memory 402 sequentially receives the outputs from basic blocks selected in the vertical direction. The two-line memory 402 outputs the signal of a basic block selected by a horizontal direction block selection line 306. Hence, only the detection signals from basic blocks selected by the vertical direction photodetector selection lines 403 selected by the vertical direction read-out block selection circuit 302, and the horizontal direction block selection lines 306, are output from the output terminal.

When the vertical direction read-out block selection circuit 302 and horizontal direction read-out block selection circuit 303 are simultaneously operated, the detection signal from an arbitrary basic block can be output from the output terminal.

As has been described above, according to the first to fourth embodiments, since photodetection signals are read from the image pickup elements in units of basic blocks, basic blocks necessary for interpolation processing are stored in the block memory, and interpolated pixels of the respective colors are obtained on the basis of the photodetection signals stored in the block memory, an interpolated signal of each color in an arbitrary region can be obtained at random.

In addition, since all signal processing operations can be performed as analog processing, the A/D and D/A converters can be omitted. Therefore, the circuit scale can be reduced.

Furthermore, since the image pickup element, block memory, interpolation circuit, and signal processing circuit can be formed on one chip by the same process, a one-chip image pickup device can be realized.

Many widely different embodiments of the present invention may be constructed without departing from the spirit and scope of the present invention. It should be understood that the present invention is not limited to the specific embodiments described in the specification, except as defined in the appended claims.

WHAT IS CLAIMED IS:

1. An image pickup element comprising:

a plurality of photodetectors each having a color filter array;

vertical direction selection means for selecting in a vertical direction an arbitrary basic block having at least two of said plurality of photodetectors;

horizontal direction selection means for selecting the arbitrary basic block in a horizontal direction; and

output means for parallelly outputting outputs from said photodetectors in the arbitrary basic block selected by said vertical direction selection means and said horizontal direction selection means.

2. An element according to claim 1, wherein a region of the basic block equals a region of a basic pattern of repeated patterns of the color filter array.

3. An element according to claim 1, wherein a region of the basic block equals a region obtained by equally dividing a basic pattern of repeated patterns of the color filter array.

4. An element according to claim 1, wherein said output means comprises selection means for selecting the basic block in the horizontal direction to output

the outputs from said photodetectors in the basic block.

5. An element according to claim 2, wherein said output means comprises selection means for selecting the basic block in the horizontal direction to output the outputs from said photodetectors in the basic block.

6. An element according to claim 3, wherein said output means comprises selection means for selecting the basic block in the horizontal direction to output the outputs from said photodetectors in the basic block.

7. An element according to claim 1, wherein

said vertical direction selection means selects said photodetectors in the selected basic block in units of lines with a time delay, and

said output means comprises storage means for storing the outputs from said photodetectors selected by said vertical direction selection means with a time delay and parallelly outputting signals from said photodetectors in the basic block.

8. An element according to claim 2, wherein

said vertical direction selection means selects

said photodetectors in the selected basic block in units of lines with a time delay, and

said output means comprises storage means for storing the outputs from said photodetectors selected by said vertical direction selection means with a time delay and parallelly outputting signals from said photodetectors in the basic block.

9. An element according to claim 3, wherein said vertical direction selection means selects said photodetectors in the selected basic block in units of lines with a time delay, and

said output means comprises storage means for storing the outputs from said photodetectors selected by said vertical direction selection means with a time delay and parallelly outputting signals from said photodetectors in the basic block.

10. An element according to claim 1, wherein the color filter array comprises a filter for transmitting only red light within a visible light range, a filter for transmitting only green light within the visible light range, and a filter for transmitting only blue light within the visible light range.

11. An element according to claim 2, wherein the color filter array comprises a filter for transmitting

only red light within a visible light range, a filter for transmitting only green light within the visible light range, and a filter for transmitting only blue light within the visible light range.

12. An element according to claim 3, wherein the color filter array comprises a filter for transmitting only red light within a visible light range, a filter for transmitting only green light within the visible light range, and a filter for transmitting only blue light within the visible light range.

13. An element according to claim 1, wherein the color filter array comprises a filter for shielding only red light within a visible light range, a filter for shielding only green light within the visible light range, a filter for shielding only blue light within the visible light range, and a filter for transmitting only green light within the visible light range.

14. An element according to claim 2, wherein the color filter array comprises a filter for shielding only red light within a visible light range, a filter for shielding only green light within the visible light range, a filter for shielding only blue light within the visible light range, and a filter for transmitting only green light within the visible light range.

15. An element according to claim 3, wherein the color filter array comprises a filter for shielding only red light within a visible light range, a filter for shielding only green light within the visible light range, a filter for shielding only blue light within the visible light range, and a filter for transmitting only green light within the visible light range.

16. An image pickup device comprising:

(A) an image pickup element including;

(a) a plurality of photodetectors each having a color filter array;

(b) vertical direction selection means for selecting in a vertical direction an arbitrary basic block having at least two of said plurality of photodetectors;

(c) horizontal direction selection means for selecting the arbitrary basic block in a horizontal direction; and

(d) output means for parallelly outputting outputs from said photodetectors in the arbitrary basic block selected by said vertical direction selection means and said horizontal direction selection means;

(B) block storage means for storing a plurality of outputs from said image pickup elements in units of basic blocks; and

(C) interpolation means for calculating an interpolated pixel on the basis of an output from said block storage means.

17. A device according to claim 16, wherein said block storage means and said interpolation means are formed on one semiconductor chip together with said image pickup element.

18. A device according to claim 16, further comprising signal processing means for performing at least one of color gain adjustment, low-frequency filtering, and edge enhancement.

19. A device according to claim 18, wherein said block storage means, said interpolation means, and said signal processing means are formed on one semiconductor chip together with said image pickup element.

ABSTRACT OF THE DISCLOSURE

To output a color image signal of an arbitrary basic block and facilitate processing on the output side, an image pickup element including a plurality of photodetectors each having a color filter array, a vertical direction selection circuit for selecting in the vertical direction an arbitrary basic block having at least one of the plurality of photodetectors, a horizontal direction selection circuit for selecting the arbitrary basic block in the horizontal direction, and an output circuit for parallelly outputting outputs from the photodetectors in the arbitrary basic block selected by the vertical direction selection circuit and horizontal direction selection circuit is provided.

FIG. 1

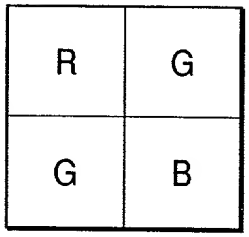


FIG. 2A

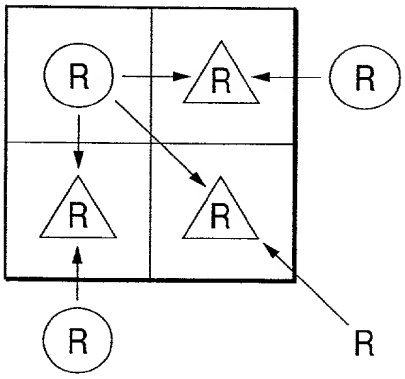


FIG. 2B

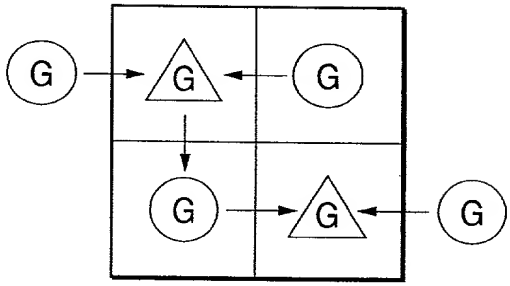


FIG. 2C

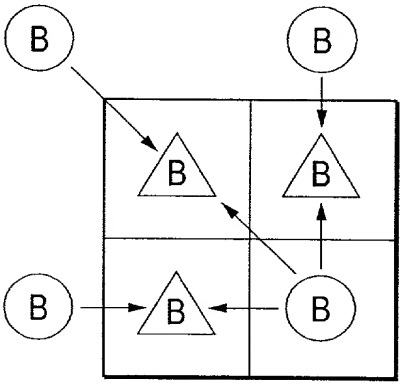


FIG. 3

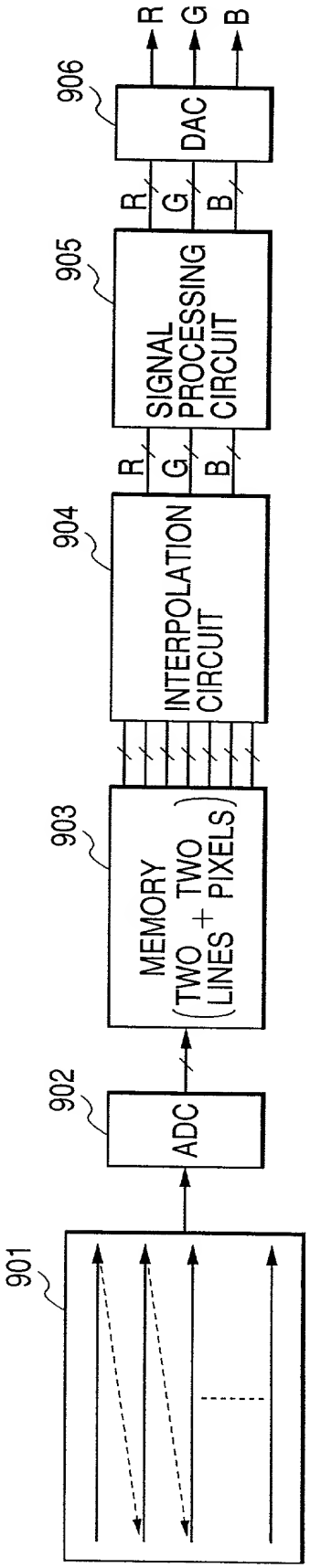

901
902
ADC
903
MEMORY
(TWO LINES + TWO PIXELS)
904
INTERPOLATION CIRCUIT
R
G
B
905
SIGNAL PROCESSING CIRCUIT
R
G
B
906
DAC
R
G
B

FIG. 4

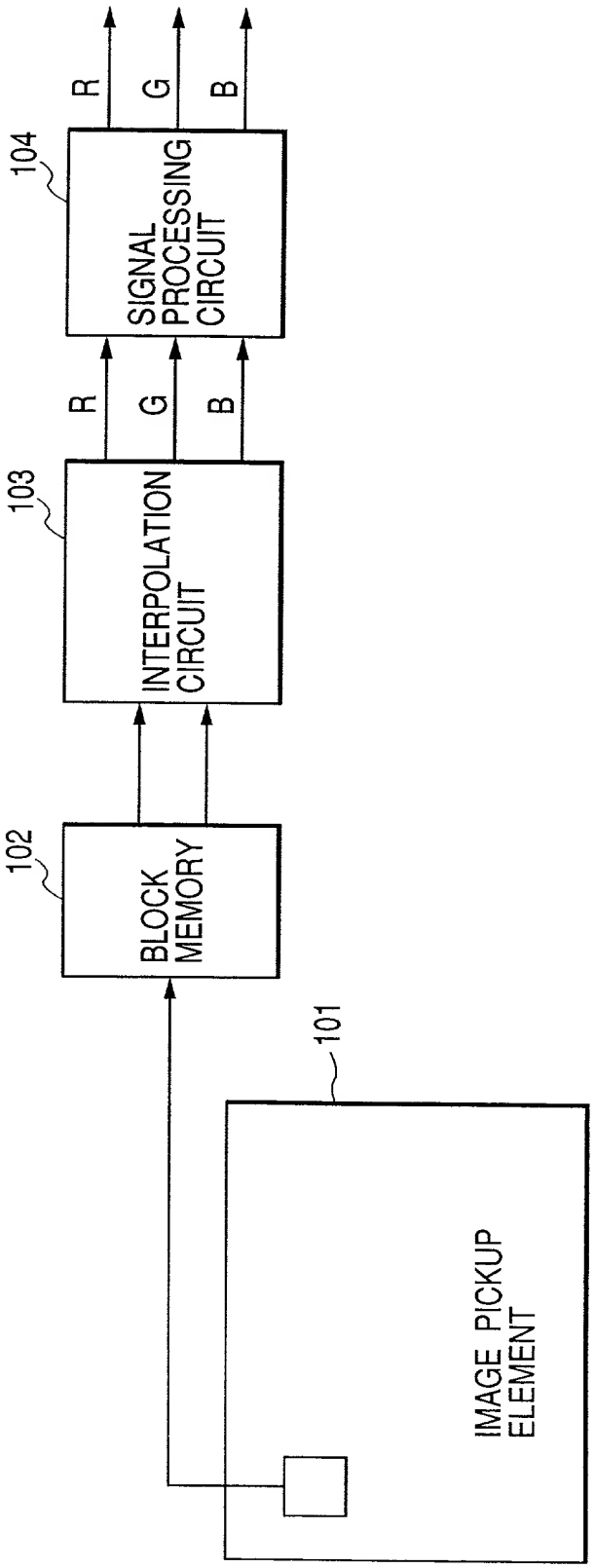


IMAGE PICKUP ELEMENT
101
BLOCK MEMORY
102
INTERPOLATION CIRCUIT
103
SIGNAL PROCESSING CIRCUIT
104
R
G
B
R
G
B

FIG. 5

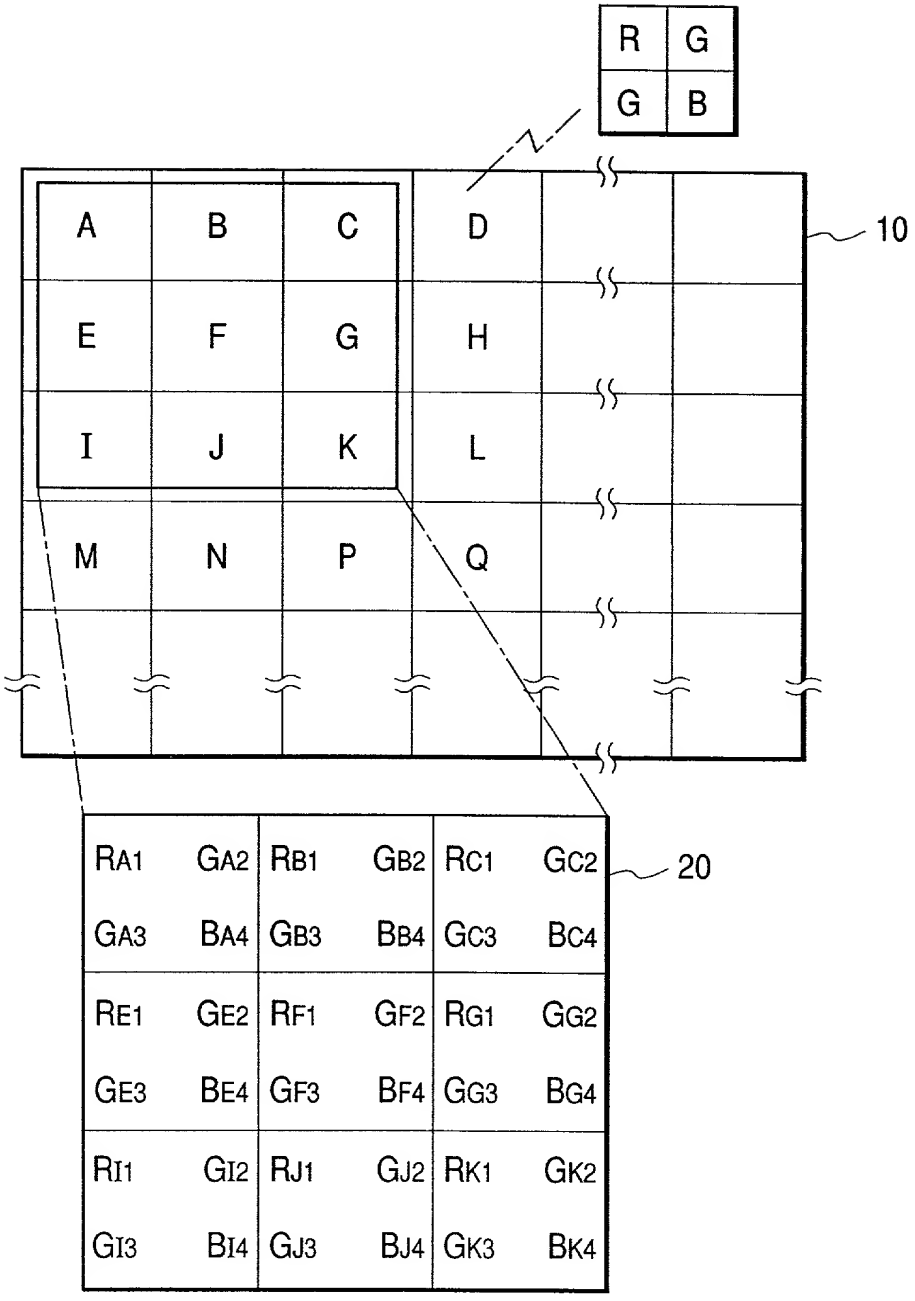

R G
G B
A B C D
E F G H
I J K L
M N P Q
10
RA1 GA2 RB1 GB2 RC1 GC2
GA3 BA4 GB3 BB4 GC3 BC4
RE1 GE2 RF1 GF2 RG1 GG2
GE3 BE4 GF3 BF4 GG3 BG4
RI1 GI2 RJ1 GJ2 RK1 GK2
GI3 BI4 GJ3 BJ4 GK3 BK4
20

FIG. 6

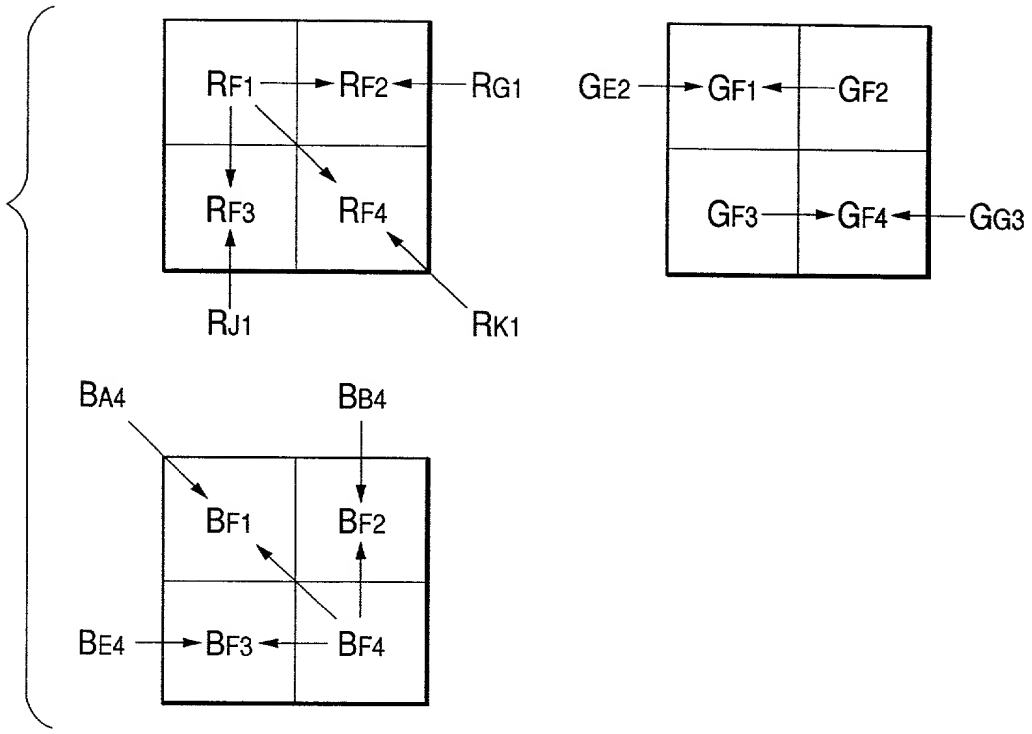

RF1
RF2
RG1
RF3
RF4
RJ1
RK1
GE2
GF1
GF2
GF3
GF4
GG3
BA4
BB4
BF1
BF2
BE4
BF3
BF4

FIG. 7

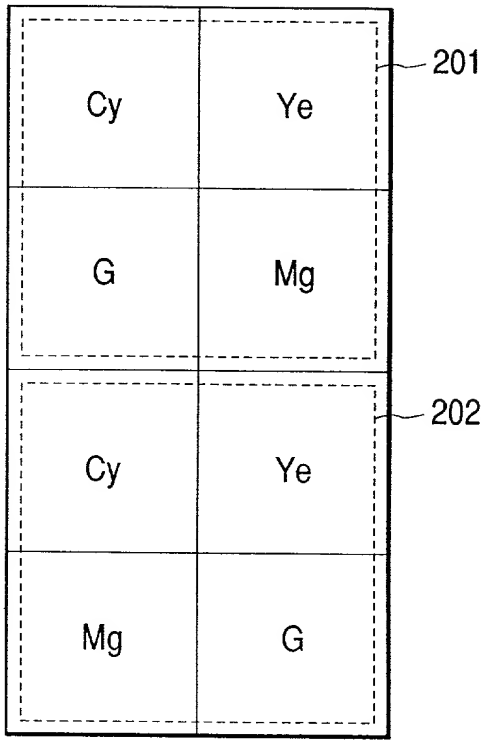

Cy
Ye
G
Mg
Cy
Ye
Mg
G
201
202

FIG. 8

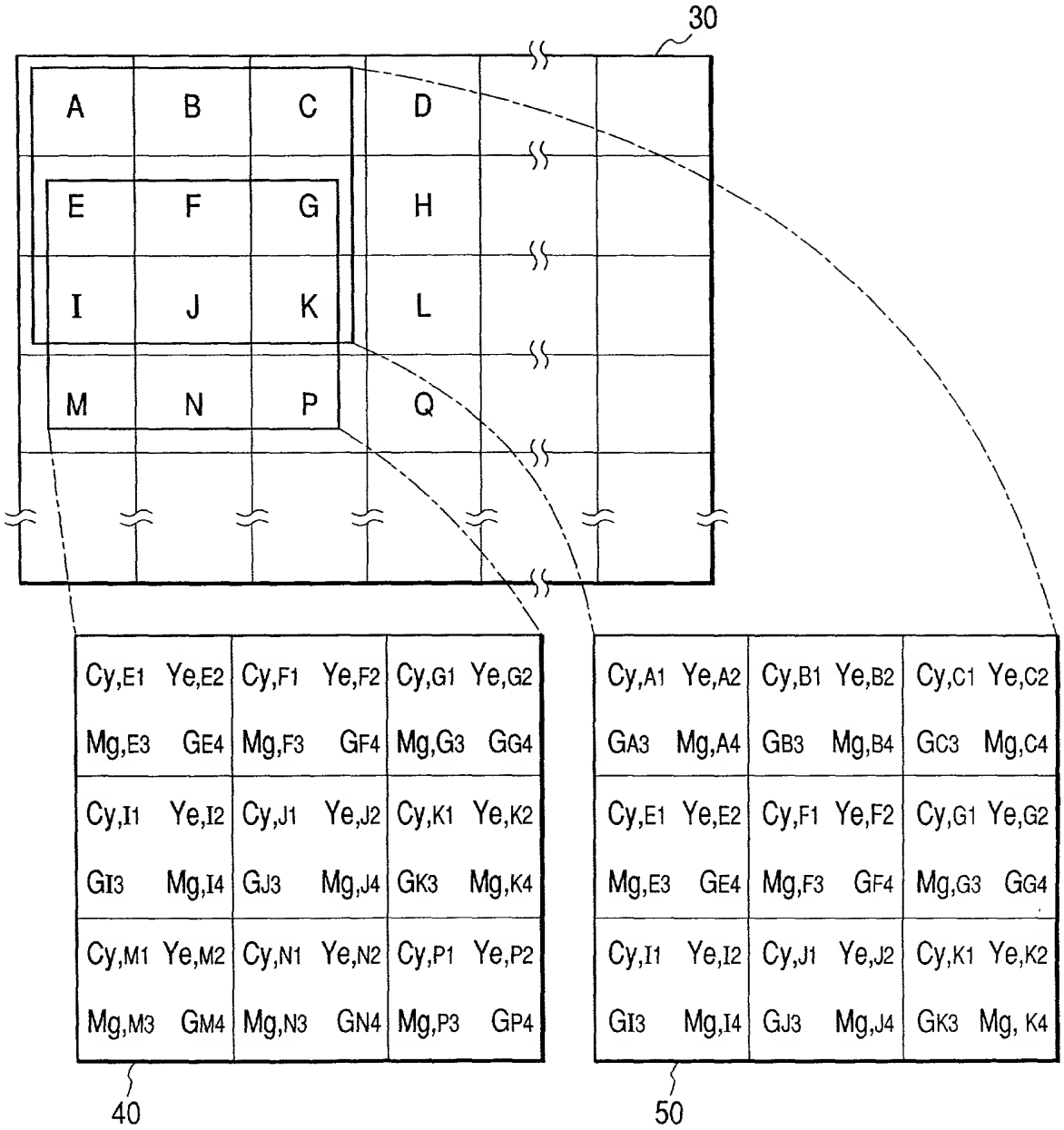

30
A B C D
E F G H
I J K L
M N P Q
Cy,E1 Ye,E2 Cy,F1 Ye,F2 Cy,G1 Ye,G2
Mg,E3 GE4 Mg,F3 GF4 Mg,G3 GG4
Cy,I1 Ye,I2 Cy,J1 Ye,J2 Cy,K1 Ye,K2
GI3 Mg,I4 GJ3 Mg,J4 GK3 Mg,K4
Cy,M1 Ye,M2 Cy,N1 Ye,N2 Cy,P1 Ye,P2
Mg,M3 GM4 Mg,N3 GN4 Mg,P3 GP4
40
Cy,A1 Ye,A2 Cy,B1 Ye,B2 Cy,C1 Ye,C2
GA3 Mg,A4 GB3 Mg,B4 GC3 Mg,C4
Cy,E1 Ye,E2 Cy,F1 Ye,F2 Cy,G1 Ye,G2
Mg,E3 GE4 Mg,F3 GF4 Mg,G3 GG4
Cy,I1 Ye,I2 Cy,J1 Ye,J2 Cy,K1 Ye,K2
GI3 Mg,I4 GJ3 Mg,J4 GK3 Mg, K4
50

FIG. 9

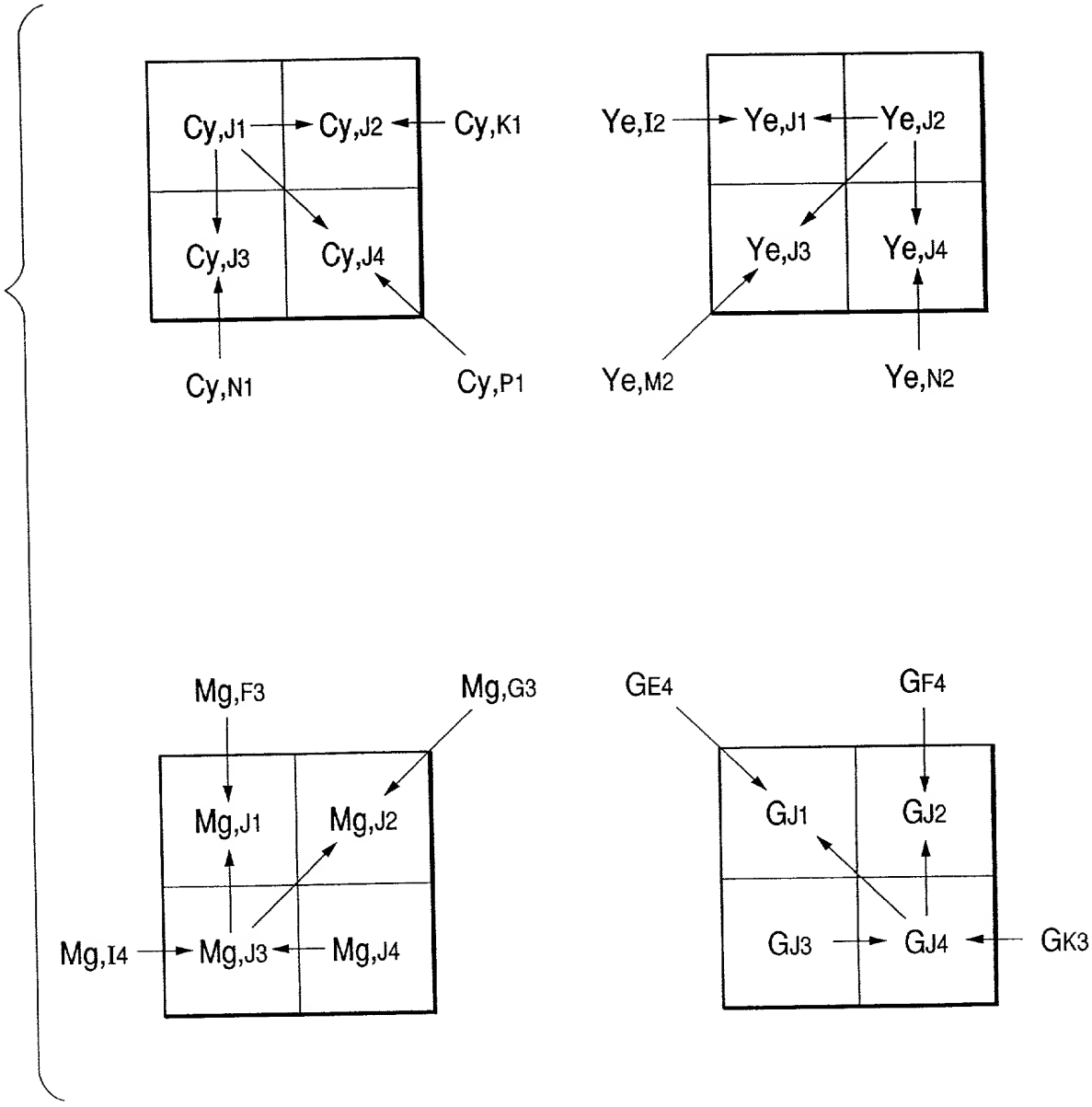

Cy,J1
Cy,J2
Cy,K1
Cy,J3
Cy,J4
Cy,N1
Cy,P1
Ye,I2
Ye,J1
Ye,J2
Ye,J3
Ye,J4
Ye,M2
Ye,N2
Mg,F3
Mg,G3
Mg,J1
Mg,J2
Mg,I4
Mg,J3
Mg,J4
GE4
GF4
GJ1
GJ2
GJ3
GJ4
GK3

FIG. 10

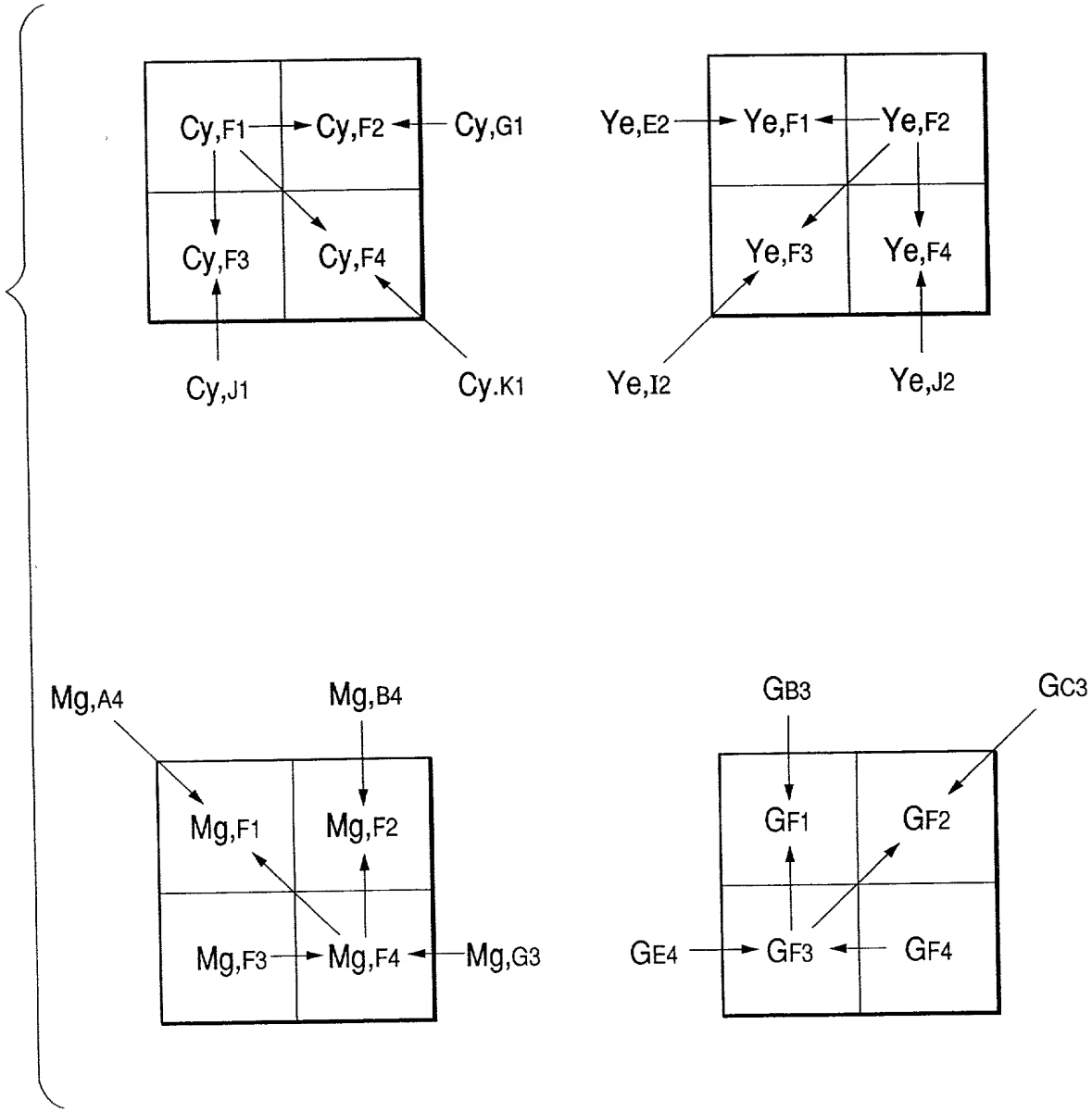

Cy,F1
Cy,F2
Cy,G1
Cy,F3
Cy,F4
Cy,J1
Cy.K1
Ye,E2
Ye,F1
Ye,F2
Ye,F3
Ye,F4
Ye,I2
Ye,J2
Mg,A4
Mg,B4
Mg,F1
Mg,F2
Mg,F3
Mg,F4
Mg,G3
GB3
GC3
GF1
GF2
GE4
GF3
GF4

FIG. 11

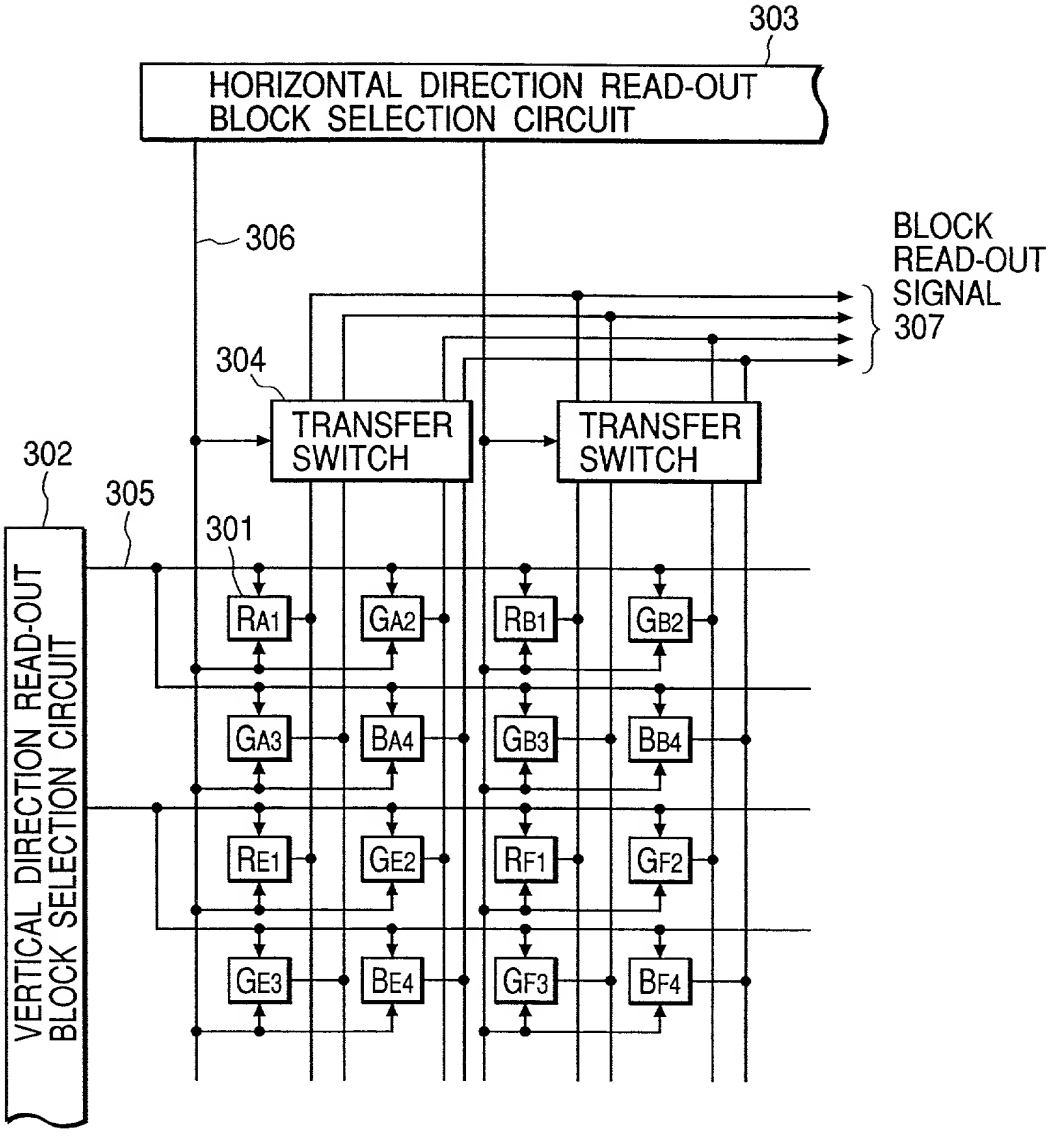
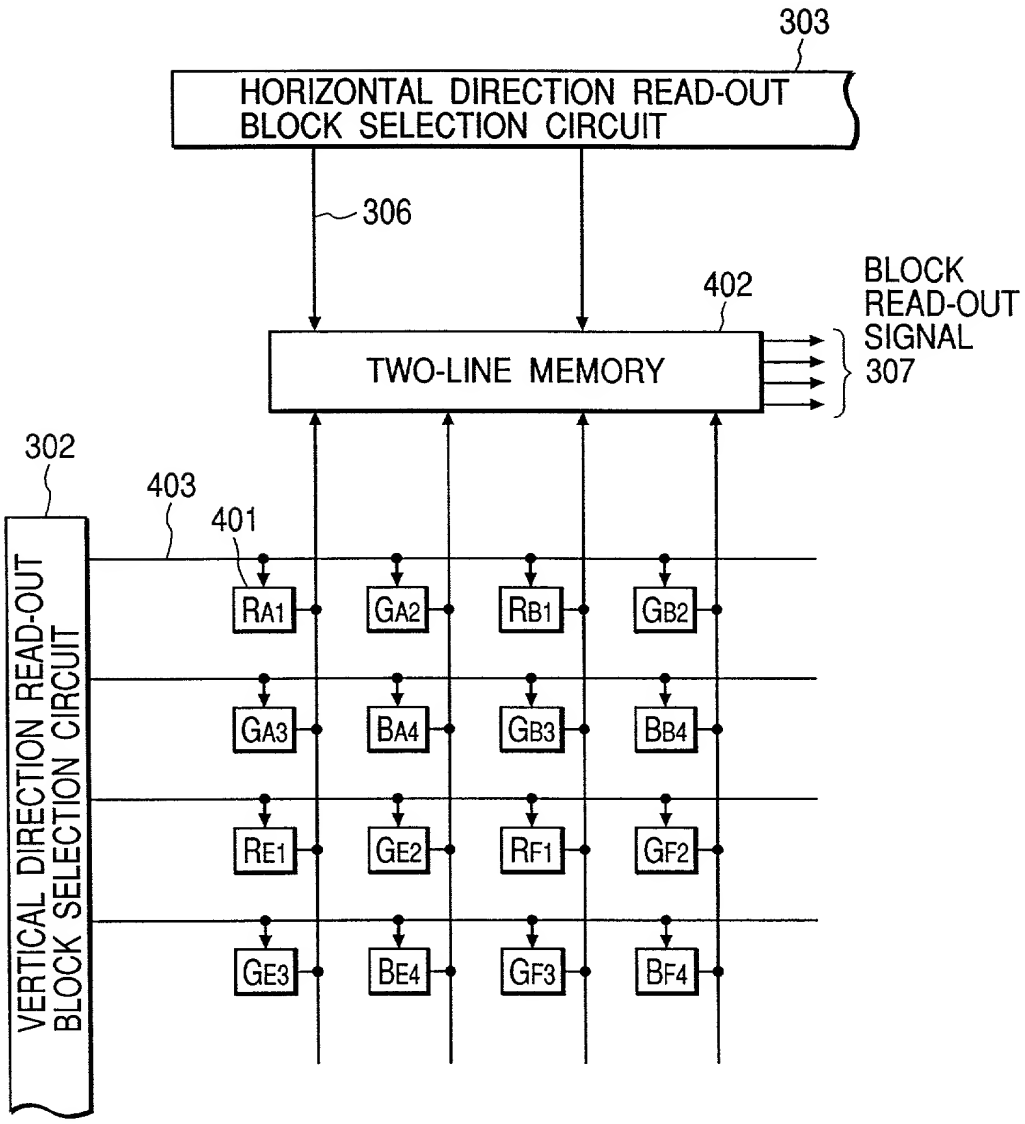

303
HORIZONTAL DIRECTION READ-OUT BLOCK SELECTION CIRCUIT
306
BLOCK READ-OUT SIGNAL 307
304
TRANSFER SWITCH
TRANSFER SWITCH
302
305
301
VERTICAL DIRECTION READ-OUT BLOCK SELECTION CIRCUIT
RA1
GA2
RB1
GB2
GA3
BA4
GB3
BB4
RE1
GE2
RF1
GF2
GE3
BE4
GF3
BF4

FIG. 12


303
HORIZONTAL DIRECTION READ-OUT BLOCK SELECTION CIRCUIT
306
402
BLOCK READ-OUT SIGNAL 307
TWO-LINE MEMORY
302
403
401
VERTICAL DIRECTION READ-OUT BLOCK SELECTION CIRCUIT
RA1
GA2
RB1
GB2
GA3
BA4
GB3
BB4
RE1
GE2
RF1
GF2
GE3
BE4
GF3
BF4

COMBINED DECLARATION AND POWER OF ATTORNEY
FOR PATENT APPLICATION
(Page 1)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled IMAGE PICKUP ELEMENT,

the specification of which [X] is attached hereto [ ] was filed on _____ as United States Application No. or PCT International Application No. _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR §1.56.

I hereby claim foreign priority benefits under 35 U.S.C. §119(a)-(d) or §365(b), of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT international application which designates at least one country other than the United States, listed below and have also identified below any foreign application for patent or inventor's certificate, or PCT international application having a filing date before that of the application on which priority is claimed:

Country	Application No.	Filed (Day/Mo./Yr.)	(Yes/No) Priority Claimed
Japan	9-361096	December 26, 1997	Yes

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s), or § 365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 C.F.R. § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

Application No.	Filed (Day/Mo./Yr.)	Status (Patented, Pending, Abandoned)

I hereby appoint the practitioners associated with the firm and Customer Number provided below to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith, and direct that all correspondence be addressed to the address associated with that Customer Number:

FITZPATRICK, CELLA, HARPER & SCINTO
Customer Number: 05514

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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COMBINED DECLARATION AND POWER OF ATTORNEY
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